REMARKS

In the above-identified Office Action, the Examiner rejected Claims 1, 6, 11 and 16 under 35 U.S.C. §102(e) as being anticipated by Nakashima. Claims 2 - 5, 7 - 10, 12 – 15 and 17 - 20 were rejected under 35 USC §103(a) as being unpatentable over Nakashima in view of Acharya et al.

Applicants have amended the independent claims (i.e., Claims 1, 6, 11 and 16) to better claim the invention. Specifically, Applicants have amended the independent claims to read:

> A method of improving performance in a multiprocessor system in which a processor has to contend with other processors for a limited number of physical interfaces to transmit data to a network comprising **(support can be found on page 1, line 22 to page 2, line 15)**:
>
> determining whether data being processed is to be transmitted from the processor of the multiprocessor system to the network **(support is on page 14, lines 20 – 22 and lines 30 - 32)**;
>
> associating a virtual Internet protocol (IP) address with a memory device in response to determining that the data being processed is to be transmitted from the processor of the multiprocessor system to the network **(support is on page 11, line 29 to page 12, line 5, page 12, lines 28 – 30, page 14, lines 23 – 25, page 14, line 32 to page 15, line 2)**; and
>
> transmitting the data from the processor of the multiprocessor system using the virtual IP address associated with the memory device as a destination IP address enabling the data to be transmitted from the processor of the multiprocessor system to the memory device **(support is**

on page 15, lines 3 – 5) , wherein the memory device contends, using a controller, for one of the limited number of physical interfaces to transmit the data to the network **(support is on page 12, lines 6 – 8)**

Further, in view of the changes to the independent claims, Applicants have also amended Claims 2, 4, 7, 9, 12, 14, 17 and 19.

For the reasons stated more fully below, Applicants submit that the claims are allowable over the applied references. Hence, reconsideration, allowance and passage to issue are respectfully requested.

The invention is set forth in claims of varying scopes of which Claim 1 is illustrative.

> 1. A method of improving performance in a multiprocessor system in which a processor has to contend with other processors for a limited number of physical interfaces to transmit data to a network comprising:
>
> determining whether data being processed is to be transmitted from the processor of the multiprocessor system to the network;
>
> associating a virtual Internet protocol (IP) address with a memory device in response to determining that the data being processed is to be transmitted from the processor of the multiprocessor system to the network; and
>
> ***transmitting the data from the processor of the multiprocessor system using the virtual IP address associated with the memory device as a destination IP address enabling the data to be transmitted from the processor of the multiprocessor system to the memory device, wherein the memory device contends, using a controller, for one of the limited number of physical interfaces to transmit the data to the network***. (Emphasis added.)

Applicants submit that the claims are patentable over the applied references.

Nakashima purports to teach a load-balancing method for a multi-processor system with a plurality of processor modules. In accordance with the purported teachings of Nakashima, the multi-processor system is assigned a virtual IP address while each processor module of the multi-processor system is assigned a real IP address. The virtual IP address is used to direct data to the multi-processor system which then determines which one of the processor modules is to handle the data. The determination can be made based on the load of each processor module in the system. That is, when a piece of data arrives at the multi-processor system (through the use of the virtual IP address), the system forwards the data to the processor module with the lightest load for processing.

The virtual IP address of the multi-processor system and the real IP address of each module are correlated and stored for easy access by a router. This allows the router to send data to the multi-processor system using the virtual IP address when the data contains the real IP address of one of the processor modules of the multi-processor system (see paragraph [0028]).

However, Nakashima does not teach, show or suggest ***transmitting the data from the processor of the multiprocessor system using the virtual IP address associated with the memory device as a destination IP address enabling the data to be transmitted from the processor of the multiprocessor system to the memory device, wherein the memory device contends, using a controller, for one of the limited number of physical interfaces to transmit the data to the network*** as in the claimed invention.

Acharya et al. teach a method of virtualizing iSCSI storage. According to Acharya et al., each physical storage device supports multiple logical units (LUNs) and each supported LUN is associated with a separate TCP port number. ISCSI commands received on a given port implicitly refer to the associated LUN. An iSCSI host addresses each logical unit of storage (LUN) with a virtual IP address and port number. Using an address translation table, a virtualization gateway rewrites the destination IP address in the header of an incoming packet

as well as the destination port number to correspond to the target physical LUN. Migration of logical units across physical storage devices is supported by changing the address translation entries at the gateway; and the gateway can be provided by a standard network router with support for address translation.

However, just as in the case of Nakashima, Acharya et al. do not teach ***transmitting the data from the processor of the multiprocessor system using the virtual IP address associated with the memory device as a destination IP address enabling the data to be transmitted from the processor of the multiprocessor system to the memory device, wherein the memory device contends, using a controller, for one of the limited number of physical interfaces to transmit the data to the network*** as in the claimed invention.

Consequently, combining the teachings of Nakashima with those of Acharya et al. does not teach the claimed invention. Hence, Applicants submit that Claim 1 and its dependent claims are allowable over the applied references. The other independent claims (i.e., Claims 6, 11 and 16) and their dependent claims, which all include the emboldened/italicized limitations in the above-reproduced Claim 1, are allowable as well. Therefore, reconsideration, allowance and passage to issue of the claims in the Application are requested once more.

Respectfully Submitted

By: _____

Volel Emile
Attorney for Applicants
Registration No. 39,969
(512) 306-7969